(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
18 October 2001 (18.10.2001)

PCT

(10) International Publication Number
WO 01/78123 A1

(51) International Patent Classification[7]: H01L 21/285, 23/532, C23C 16/06, 16/44

(21) International Application Number: PCT/KR01/00605

(22) International Filing Date: 11 April 2001 (11.04.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
2000/18804 11 April 2000 (11.04.2000) KR
2000/26640 18 May 2000 (18.05.2000) KR

(71) Applicant *(for all designated States except US)*: GENITECH CO., LTD. [KR/KR]; 1694-5 Sinil-dong, Taedok-gu, Taejon 306-230 (KR).

(72) Inventor; and
(75) Inventor/Applicant *(for US only)*: PARK, Hyung, Sang [KR/KR]; Hyundai Prime Apt. 3-1306, Gu-ui 3-dong, Gwangjin-gu, Seoul 143-203 (KR).

(74) Agent: CHU, Sung, Min; Seoul Building, 114-31, Uni-dong, Chongro-gu, Seoul 110-350 (KR).

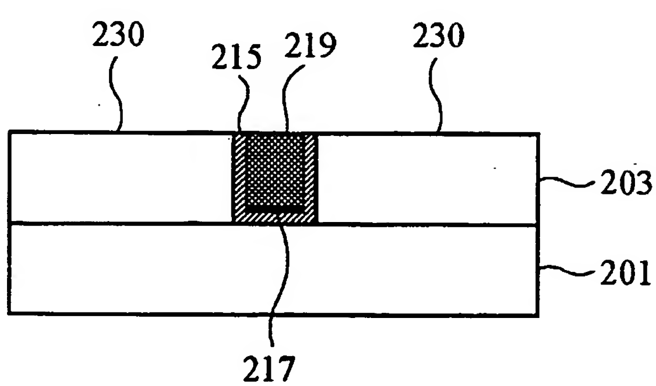
(81) Designated States *(national)*: JP, US.

(84) Designated States *(regional)*: European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: METHOD OF FORMING METAL INTERCONNECTS



(57) Abstract: A noble way of forming metal conductors for interconnecting active and passive elements as well as signal and power lines for circuits and devices on a silicon substrate is disclosed. The method disclosed herein is based on the use of copper chemical vapor deposition (CVD) process using Iodine or Iodine containing compounds as a catalyst-surfactant. The catalyst-surfactant Iodine has a property of being a good catalyst for copper metal surfaces while it is not easily adsorbed onto a surface of insulation layer as well as a diffusion barrier layer, thereby the amount of copper deposition on the insulation layer as well as the diffusion barrier layer is non-existent. By utilizing these properties, a simple and noble way of selectively depositing copper onto trenches, via holes, and contact holes from bottom up in order to form copper interconnects for primarily wiring purposes on a silicon substrate is disclosed.

WO 01/78123 A1

METHOD OF FORMING METAL INTERCONNECTS

TECHNICAL FIELD

The present invention relates to a method of forming interconnecting conductors on a semiconductor substrate by means of copper chemical vapor deposition (CVD) method using catalyst-surfactants.

BACKGROUND ART

Design rules of circuit layouts on a silicon substrate are becoming tighter and tighter as the demand for high density circuits continue increasing. As more and more circuits are to be laid out on a unit area, interconnecting active elements such as transistors, passive elements such as capacitors and resistors, as well as signal and power lines are becoming complex and difficult. Tighter design rules mean narrower metal lines. In order to maintain certain performance level of the circuits, RC time delay has to be minimized. However, the resistance of commonly used aluminum or aluminum alloys increases as the width of the interconnecting wires are becoming narrower and narrower. As a result, it is becoming difficult to maintain certain level of circuit performance by using aluminum and aluminum alloys as the interconnecting metal wires.

Recently, copper has been used for interconnecting metal wires instead of aluminum and aluminum alloys. Since copper has higher conductivity than aluminum, the circuit performance degradation problem due to long RC time delay can be solved by using copper as a wiring metal for interconnection.

Copper may be etched using wet etching method, but it is very difficult to etch copper material by means of dry

etching method, thereby it is not an easy task to perform selective etching on copper compared to aluminum.

Therefore, unlike the interconnect process using aluminum where the entire surface area of a substrate is covered with a thin layer of aluminum and then selectively etching the unnecessary areas to complete the necessary wiring, such a method can not be used with copper. Instead, after forming an insulation layer and etching off unnecessary areas in order to make trenches and via holes, only these trenches and via holes are filled with copper in order to create and complete interconnecting wires and connectors. This method is known as damascene or inlay process.

Klaus D. Beyer, et al. (US Patent No. 4,944,836) discloses a method for producing coplanar metal insulator films on a substrate according to a chemical-mechanical polishing (CMP) technique. One example given therein is that a substrate having a patterned insulating layer of dielectric material thereon, is coated with a layer of metal. The substrate is then placed in a parallel polisher and the metal is removed elsewhere, except in the holes where it is left intact. This is made possible through the use of an improved selective slurry which removes the metal much faster than the dielectric material. The insulating layer is then used as an automatic etch stop barrier. Another example given therein is that a substrate having a patterned metallic layer is coated with an insulating layer and then subject to chemical-mechanical polishing. The structure is coplanarized by the chemical-mechanical removal of the insulating material from the high points of the structure at a faster rate than from the lower points.

Electrochemical deposition, also known as electroplating technique, is a widely used copper fill technology. The electroplating technique known as EP has drawbacks. First drawback is that a conductive seed layer for use as an electrode must be formed by other means before copper is deposited or filled by using this electroplating

technique. Second one is that selective deposition of copper is not possible because copper layer must be formed only on the surfaces covered with conductive seed layers, and the object of the present invention is to selectively deposit copper film layer or patterned depressions on a substrate. The depressions include trenches, via holes and contact holes. Third drawback is that a substrate must be cleaned thoroughly using highly purified DI water in order to remove the harsh chemicals used during the electroplating process, whereas conventional physical vapor deposition (PVD) method or chemical vapor deposition (CVD) method do not require such laborious and costly operation.

The physical vapor deposition method such as sputtering technique has a process characteristics so called line of sight deposition, whereby deep trenches and holes with respect to a top opening, that is, trenches and holes with high aspect ratio, are filled the top openings first, thereby creating pinch-offs or voids before the inside of trenches and holes are filled.

Therefore, it is very difficult to selectively fill the interior portion of trenches and holes by using sputtering technique when the top openings are significantly smaller than one micron in width.

Furthermore, even when conventional chemical vapor deposition (CVD) method is used, a metal layer with uniform thickness is deposited on the surface of an insulating layer following the contour of its uneven surface. As metal film layers grow the film layers growing on the sidewalls meet inside the trenches and holes and as a result a seam is created at the interfacing surface boundary of such film layers inside a trenches or a hole, which seam contains micro-voids created by minutely detailed surface roughness. Such micro-voids are very difficult to control and suppress.

However, since a metal film is formed by means of chemical vapor deposition (CVD) where the chemical reaction occurs on the surface of a substrate, it is possible to carry

out, by using a CVD method, certain chemical reaction selectively only on the surface of a substrate, on which surface a few source materials are exposed.

Therefore, aforementioned micro-voids can be avoided by controlling the growth of a film on the sidewalls and by forming a metal film in one direction (upward) from the bottom-up when a CVD method is employed for filling trenches and via holes on a substrate.

Korean Patent Application No. 98-53575 discloses a method of a forming copper film by means of chemical vapor deposition method using catalyst-surfactant whereby the catalyst accelerates copper film deposition rate without being consumed during the chemical reaction or buried under the copper film being formed and said catalyst floats on the surface of the copper film being formed. Not only the copper film deposition rate of this copper CVD method using catalyst-surfactant is several tens to several hundreds times faster than conventional CVD method using same kinds of copper source materials, but also the chemical reaction of said copper CVD using catalyst occurs at a temperature as low as 100 °C. Also, by using said method, a method of forming metal interconnects by filling trenches, via holes and contact holes without creating voids therein is disclosed in the Korean Patent Application No. 2000-1232. In said invention, one of the reasons of having a faster deposition rate inside trenches, via holes and contact holes is because the surface area decreases in view of the geometry as a copper film continue formed, thereby the density of the catalyst at the surface of a copper film layer increases, and as a result the copper film deposition rate increases in proportion to the surface area of the copper film that is being formed. However, even if said invention is used, it is necessary to suppress the copper film growth on the sidewalls of trenches, via holes and contact holes when top openings of trenches, via holes and contact holes are very small. This is because, in case of large aspect ratio, it is quite possible that even a slow

growing copper film on the sidewalls may grow too fast and close the top openings before trenches, via holes and contact holes are filled from bottom up.

Vaporized source materials for use with the coppers CVD method using catalyst have different adsorption and decomposition characteristics depending upon the properties of the metals and dielectrics already formed on a substrate.

Therefore, it is possible to form copper film layers selectively by using the copper CVD method using catalyst when the substrate contain different materials such as metals and dielectrics where copper deposition occurs in certain areas more easily, because of better adsorption and decomposition characteristics of the source materials in relation to the materials in those areas than in other areas on the substrate because of poor adsorption and decomposition characteristics of the source materials in relation to the materials in those other areas.

By using aforementioned characteristics of the catalysts for the metal CVD method using catalyst, deposition and growth rate of metal formation on a substrate can be controlled depending upon the materials used on the substrate along with the catalyst used.

This leads to the present invention where by utilizing the characteristics of the catalysts used, trenches, via holes and contact holes can be filled with metal film layers without creating either voids or seams. The method disclosed here, according to the present invention, can be applied to metal interconnects for interconnecting semiconductor elements as well as liquid crystal display (LCD) elements.

DISCLOSURE OF THE INVENTION

A method of forming metal interconnects without creating voids and seams by filling trenches, via holes as well as contact holes patterned on a substrate is disclosed

according to the present invention. In the Preferred Embodiments, to be described in the following, of the present invention, a metal CVD(chemical vapor deposition) method using catalyst-surfactant is utilized as a means of depositing metals as well as selectively forming interconnecting metal layers.

In the Embodiments presented here, Iodine is used as a catalyst-surfactant and copper is the interconnection metal. When Iodine or Iodine containing compounds are used as catalyst-surfactant, their adsorption and decomposition characteristics are very different depending upon the surfaces they are treated on. Such catalysts are adsorbed well onto a metallic surface and stays on the surface areas. But they are not adsorbed onto the surface of insulation layers and diffusion barrier layers. Furthermore, the reaction temperature of a metal CVD using catalyst-surfactant is significantly lower than that of a CVD without using catalyst-surfactant. The metal CVD using catalyst-surfactant has a very high deposition rate at lower temperatures compared to the deposition rate of metal CVD without using catalyst-surfactant at high temperatures.

By using these very different characteristics between a seed layer and insulation layer as well as diffusion barrier layer in terms of adsorption and decomposition of catalyst-surfactant, the copper film deposition rate on a surface and the reaction temperature of copper and catalyst-surfactant, a selective deposition of copper on the seed layer only in the trenches, via holes and contact holes is possible, thereby a patterned metal layer is formed according to the present invention. Since the catalyst-surfactant floats on the metallic surfaces as the metallic film layer being formed, the copper deposition rate is accelerated as the copper film layer continue growing in the trenches and holes, for example. Meanwhile, copper does not deposit on the surface of an insulating layer or on the surfaces of the sidewalls of trenches and holes where there

is no seed layer. Also, copper does not deposit on the surface of a diffusion barrier layer without a seed layer according to the present invention.

Another result of the present invention is that since a copper film layer grows much faster on the surface of a seed layer at the bottom of trenches and holes and it grows much slower on the sidewalls of trenches and holes of which sidewalls are without seed layers, the copper film layer grows from bottom up without creating voids, seams and pinch-offs in trenches, via holes and contact holes according to the present invention. Therefore, an effective formation of copper interconnects is possible, and a method thereof is disclosed here.

According to the present invention, Iodine and Bromine and their compounds which elements are belonging to the Halogen group can be used as catalysts, as disclosed in Korean Patent Application No. 98-53575, in depositing metals by using the copper CVD method using catalyst-surfactant, where the catalysts are not buried under a metal film being formed and rather the catalysts float on the surface of a metal film being formed, thereby the catalysts continue accelerating the metal film formation process, thereby increasing the metal film deposition rate.

According to the present invention, when Iodine is supplied in the form of Iodoethene(C_2H_5I), on the surface of a metal belonging to the transition metal group such as copper, Iodine adsorbs better onto a copper surface and it accelerates the copper deposition reaction, but Iodine does not work as a catalyst on a surface of Tantalum Nitride(TaN) or Silicon Dioxide(SiO_2).

As a method of metal interconnecting of semiconductor elements, copper interconnect has been recently getting attention in conjunction with damascene processes, where trenches and via holes are etched out of an insulation layer, and thereon a copper layer is deposited in order to fill trenches and via holes.

According to the present invention, in order to selectively deposit metal onto metal interconnecting structures such as trenches, via holes and contact holes on a substrate, a seed layer using a transition metal family of metals such as copper that has a characteristics of good adsorption and decomposition so that a catalyst can be easily adsorbed onto the surface of the bottom part of trenches, via holes and contact holes, the catalyst can help copper source material react actively for fast deposition, is formed. The sidewalls of trenches, and via holes and contact holes are covered as diffusion barrier layer with such material as Tantalum Nitride(TaN) which material has a characteristics of poor adsorption and decomposition so that the metal film layer would not be formed fast on the sidewalls. Furthermore, the copper CVD method using catalyst-surfactant is operated at a much lower temperature than a normal CVD requires so that a metal film layer is formed much faster at the bottom of trenches, via holes and contact holes than sidewalls, and thereby trenches, via holes and contact holes are filled from bottom up fast. The operating temperature of a normal CVD method is about 180 °C or higher, whereas the operating temperature of a copper CVD method using catalyst-surfactant is as low as 50 °C and the normal range of the operating temperature is 100 °C ~ 150 °C. However, the deposition rate for the copper CVD method using catalyst is several times to several 10 tens times faster than a normal CVD method.

According to the present invention, metal interconnects are formed by selectively depositing metal film layers on the trenches, via holes and contact holes on a substrate by means of a metal CVD method using catalyst-surfactant.

BRIEF DESCRIPTION OF THE DRAWINGS

Following figures describe, in steps, the procedures

in accordance with the present invention.

Fig. 1A is a cross-sectional drawing showing a patterned insulation layer.

Fig. 1B is a cross-sectional view of a diffusion barrier layer added to the step in Fig. 1A.

Fig. 1C is a cross-sectional view of a selectively formed seed layer added to the diffusion barrier layer of Fig. 1B.

Fig. 1D is a cross-sectional view of a metal layer added to the seed layer of Fig. 1C, formed after the surface in Fig. 1C is treated with a catalyst.

Fig. 2A is a cross-sectional view of Fig. 1C after removing the diffusion barrier layer and the seed layer from the top flat surface in Fig. 1C.

Fig. 2B is a cross-sectional view of Fig. 2A after a metal layer is formed from the top.

MODES OF CARRYING OUT THE INVENTION

Following Preferred Embodiments will clarify the basic principles of the present invention.

PREFERRED EMBODIMENT 1

In accordance with the present invention, a method of forming metal interconnects for fabricating semiconductor integrated circuits is disclosed. The interconnecting metal conductor fabrication process using trenches and via holes

consists of the following six steps : (1) a step of forming a pattern of insulating layer (Fig. 1A), (2) a step of forming a conductive diffusion barrier layer on top of said patterned insulation layer (Fig. 1B), (3) a step of forming a seed layer that adsorbs catalysts well by means of anisotropic deposition on top of said diffusion barrier layer excluding the sidewalls (Fig. 1C), (4) a step of forming a layer of catalyst only on the flat surfaces consisting of flat top area and the bottom area of trenches and via holes of said seed layer (Fig. 1D), (5) a step of filling said trenches and via holes in a bottom-up fill fashion by means of a chemical vapor deposition (CVD) method on the flat horizontal surfaces treated with catalysts, (Fig. 1D), (6) a step of forming a pattern of metal layer by removing said metal layer formed in step (5) above with the exception of said metal layer filling the trenches and via holes (Fig. 1E).

The interconnect fabrication process for contact holes with diffused bottom surfaces consists of seven steps, of which six steps are the same as for trenches and via holes aforedescribed, and one additional step is added between the step (1) and the step (2). This additional step is necessary for reducing the contact resistance by forming refractory metal film layers, such as Tantalum (Ta) and Tantalum Nitride(TaN).

The material that may be used as catalysts are again Iodine (I) and Bromine (Br) and their compounds. For example, Iodine (I) and Iodine containing compounds such as iodoethane (C_2H_5I), iodomethane(CH_3I), diiodomethane(CH_2I_2) or trifluoroiodomethane(CF_3I), may be used as catalysts in conjunction with a copper metal source material Cu(I)-hexafluoroacetylacetonate vinyltrimethyl silane (hfac)Cu(vtms) by means of the copper chemical vapor deposition (CVD) method using catalysts in forming metal interconnects.

The materials that may be used as seed layers are a metal group consisting of copper (Cu), Titanium (Ti), Gold(Au),

Silver(Ag), Palladium(Pd), Tungsten(W), Platinum(Pt) and Aluminum(Al), or a combination of one or more elements of the above.

In this preferred Embodiment 1, detailed steps of a method of selectively forming copper interconnects by using structures of trenches, via holes and contact holes by means of the copper CVD method using Iodine as a catalyst are described in the following according to the present invention.

In describing a method of forming metal interconnects here, repeated explanations of the processing steps are avoided wherever possible, and also same item numbering system is used for all drawings in order to simplify explanations.

Referring to Fig. 1A, an insulation layer 103 is formed on a substrate 101 first, and then by means of etching process, a pattern of trenches 120 and via holes 120 or contact holes 120. The item number 120 is used for both trenches, and via holes as well as contact holes for the purpose of describing the steps of forming metal interconnects using cross-sectional drawings. In case of a contact hole, the substrate 101 may be a silicon substrate that contains n-type or p-type of impurities. On the other hand, if the hole is a via hole 120, there would be another insulation layer (not shown) between the insulation layer 103 and the substrate 101, where such insulation layer (not shown) may contain patterned metal interconnects, and also there may be a non-conducting diffusion barrier layer between those two insulation layers which diffusion barrier layer plays a role of etch-stop as well as blocking metal diffusions into insulation layer 103 or the substrate 101. As an example, in case of copper interconnects, via holes and trenches may be formed by performing the steps of forming a silicon Nitride (Si_3N_4) film layer first and then etching it to form a pattern.

Next step is to form a conductive diffusion barrier layer 105. Referring to Fig. 1B, a diffusion barrier 105 is

formed by means of a chemical vapor deposition (CVD) method or an atomic layer deposition (ALD) method in order to prevent an interconnecting metal or a seed layer (not shown yet) (107 in Fig. 1C) from being diffused into the substrate 101 or the insulation layer 103. Said diffusion barrier layer 105 is formed by using preferably Tantalum Nitride (TaN), or Titanium Nitride (TiN) onto which said catalyst are not easily adsorbed, thereby they do not accelerate the metal film formation, and also these diffusion barrier layer materials have a long incubation time period necessary for forming metal film layers. Uniform thickness of a diffusion barrier layer following the contour of trenches and holes is desired.

Meanwhile, if contact holes are to be filled, the contact resistance must be lowered and also in order to make a good ohmic contact, an ohmic metal layer using low resistivity metals such as Titanium(Ti) and Cobalt(Co) may be formed before a diffusion barrier layer is formed (not shown). It is desirable to anneal said refractory metal (Ti and Co) film layers during which a silicide layer is formed at the boundary through the chemical reaction of the impurities with silicon.

Next step is to form a seed layer. Referring to Fig. 1C, the flat top part and the flat bottom part of the trenches and via holes on a patterned insulation layer 103 made of oxides such as silicon oxides, a seed layer at the flat top surface 107 and a seed layer at the bottom flat part inside the trenches and via holes 117 are formed, where the thickness of the seed layer ranges from several to several hundred angstroms(Å). In order to minimize deposition of the seed layer metal onto sidewalls, sputtering apparatus equipped with a collimater is used to enhance the property known as "line-of-sight" sputtering, thereby achieving a high rate of deposition of a metal at the flat bottom part of the trenches and via holes, and virtually no deposit of metal on the sidewalls. As a result, a seed layer with discontinuities as shown in Fig. 1C is formed. If necessary, the sidewalls

may be formed in such a way that the bottom part is somewhat wider than the top opening of the trenches and via holes, so that the formation of a seed layer is controlled much better. Furthermore, deposition of a seed layer on the sidewalls can be controlled even better by following the procedure described below.

First of all, as aforedescribed, a seed layer is formed by means of anisotropic deposition, and then the resultant sidewalls are etched by means of isotropic ion etching method so that the metal film formed on the sidewalls can be etched away. If this process is repeated several times, a seed layer can be formed with the desired thickness without depositing the seed layer metal on the sidewalls.

A seed layer 107, and a seed layer 117 may be formed using the metal group such as copper(Cu), Titanium(Ti), Gold(Au), Silver(Ag), Palladium(Pd), Tungsten(W), Platinum(Pt), or Aluminum(Al), and the alloys containing one or more elements listed above. Such metals listed above react very well with catalysts listed elsewhere in this Embodiment in terms of the characteristics of good adsorption and decomposition in such away that the catalysts increase the metal deposition rate.

Referring to Fig. 1D, said resultant seed layer is treated with catalysts. For example, Iodine is used as a catalyst and copper is used as a metal film layer source material for metal interconnection. Treatment of the catalyst Iodine is carried out the same way as a chemical vapor deposition (CVD) method. Even though it is not shown in Fig. 1D, the catalyst Iodine is adsorbed much better onto the seed layer 107, but the catalyst Iodine is not adsorbed relatively well on the sidewalls where the diffusion barrier layer 105 is exposed. During the operation of a CVD, the reaction temperature is set between the temperature at which a CVD method using Iodine produces sufficiently high deposition rate and the temperature at which the metal source material decomposes by itself when a CVD method is used without Iodine.

Then, a copper film layer 109 is formed selectively by supplying Cu(I)-hexafluoroacetylacetonate vinyltrimethylsilane [(hfac)Cu(Vtms)] into a CVD apparatus.

Since the seed layer is already treated with the catalyst Iodine, a copper film layer is formed mostly on the seed layer (flat top) 107 and the seed layer (flat bottom) 117. In this case, the formation of a metal film layer occurs from bottom up because the growth of a metal film layer from sidewalls was best controlled. Therefore, even when the top opening of the trenches and via holes are small, copper material filled the trenches and via holes without creating voids or seams. Also, when the sidewalls are made of the material that the catalyst Iodine is adsorbed onto the sidewalls, but the catalyst does not function as such very well, the metal film deposition rate on the seed layer 117 at the bottom of trenches and via holes accelerate as metallic films grows. This is because the catalyst material adsorbed onto the surface of sidewalls moves onto the growing metal film, thereby this additional migrant catalyst increases the density of the catalyst-surfactant. Therefore, the metal growth rate inside the trenches and via holes is faster than the metal film growth rate on the seed layer 107 residing on the flat surface of the insulation layer 103. As a result, after certain time period of deposition, the metal film deposited on the substrate forms fairly flat metal film surface 109 as shown in Fig. 1D according to the present invention. After a metal film layer is formed, an annealing process is carried out in order to enhance the adhesion characteristics between the metal film layer 109 and the diffusion barrier layer 105 in accordance with the present invention.

The final step is to polish the metal film layer 109 to form a metal interconnect pattern. Referring to Fig. 1E, the metal film layer 109 formed in the previous process is polished by means of a polishing method such as chemical-mechanical polishing (CMP) in order to form a

pattern of metal film layer 119. During this step, the insulation layer 103 is completely exposed and only the metal layer 119 and a small portion of diffusion barrier layer 115 remains, thereby a good interconnecting metal channel is formed according to the present invention.

PREFERRED EMBODIMENT 2

According to the present invention, as Preferred Embodiment 2, the steps associated with Fig. 1A though 1C are repeated here first. Then, only the portion of the seed layer 107 and the diffusion barrier layer 105 in Fig. 1C on the flat part of the surface of the substrate are removed, resulting in trenches or via holes with a seed layer only at the bottom 217 and also the diffusion barrier layer 215 on the sidewalls and also at the bottom. In this case, the subsequent step of CMP necessary for removing the first three layers 109, 107 an 105 on the surface in Fig. 1D is eliminated, and a metal film layer formation on the flat surface of the insulation layer 103 in Fig. 1E is suppressed.(For the Preferred Embodiments, trenches, via holes and contact holes are collectively called depressions.)

In eliminating the top flat portion of the seed layer 107, and that of the diffusion barrier layer 105, it is desirable to use a slurryless CMP method in order to avoid undesirable contamination of the trenches and via holes with small polishing particles, according to the present invention. To complete the process of forming metal interconnects, in accordance with the present invention, referring to Fig. 2B, the seed layer 117 at the bottom of trenches and via holes is treated with catalyst Iodine, and then trenches and via holes are filled with copper material by means of the copper CVD method using catalyst-surfactant, and the final result is a copper film layer 219 as shown in Fig. 2B.

During copper fill, only trenches and via holes are

filled from bottom up, but no copper deposition on the top flat surface 230 of the insulation layer 203. The reasons are primarily two fold, similarly to the descriptions given in Preferred Embodiment 1. First is that copper does not deposit on the flat top surface 230 of the insulation layer 203, because the catalyst Iodine does not adsorb onto the top flat surface 230, thereby copper is not deposited on the top flat surface 230. Second is that trenches or via holes 219 are filled from bottom up due to the catalyst Iodine adsorbed onto the seed layer 217 accelerates copper deposition at a low temperature in the range of 100 °C to 150 °C, thereby the copper CVD method using Iodine accelerates the copper deposition process, but copper is not deposited onto the flat top surface 230 due to lack of catalyst Iodine. Combining the lack of catalyst Iodine and low operating temperature for copper CVD using catalyst Iodine will prohibit copper deposition on the top flat surface 230 without catalyst Iodine on it according to the present invention.

In the Preferred Embodiments described above, some of the exemplary methods of metal interconnects in realizing the present invention are disclosed and presented herein. However, those who are knowledgeable in the art should be able to easily derive other methods within the principle of the present invention. Therefore, the scope of the methods disclosed here in accordance with the present invention is not limited to the Preferred Embodiments described and presented here.

What is claimed is :

1. A method of forming metal interconnects comprising the steps of and in the order of;

forming an insulation layer on a top surface of a substrate;

forming a pattern of depressions in said insulation layer by etching;

forming a seed layer on the entire surface of said patterned insulation layer, but suppressing the formation of a seed layer on the sidewalls of said depressions;

treating a catalyst-surfactant on said surface of said seed layer;

forming a metal layer on said patterned seed layer and said depressions by means of metal chemical vapor deposition (CVD) method using catalyst-surfactant; and

forming a patterned metal layer on said depressions by removing a thin metal layer from the top surface of said substrate until a top flat part of said patterned insulation layer is exposed.

2. The method of claim 1, in which a diffusion barrier layer on said patterned insulation layer is formed before said seed layer is formed.

3. The method of claim 1 or 2, in which an adhesive metal layer is formed on said insulation layer or diffusion barrier layer or both before said seed layer is formed.

4. The method of claim 1, in which said depressions include contact holes.

5. The method of claim 1, in which said depressions include via holes.

6. The method of claim 1, in which said depressions include

trenches.

7. The method of claim 1, in which said depressions include compound structures consisting of contact holes and trenches.

8. The method of claim 1, in which said depressions include compound structures consisting of via holes and trenches.

9. The method of claim 2, in which a refractory metal layer in formed on said patterned insulation layer before said diffusion barrier layer is formed.

10. The method of claim 1, in which an anisotropic deposition is used in forming said seed layer in order to suppress deposition on the sidewalls of said patterned depressions.

11. The method of claim 10, in which a sputtering apparatus equipped with a collimator is used as a means of said anisotropic deposition method.

12. The method of claim 1, in which in forming said seed layer an anisotropic deposition method and an isotropic etching method are repeatedly used at least once.

13. The method of claim 12, in which a collimated sputtering process is used as a means of said anisotropic deposition method.

14. The method of claim 1, in which during the process of forming said patterned metal layer, a chemical-mechanical polishing (CMP) method is used.

15. The method of claim 1 or 2, in which, in order to enhance the adhesive characteristics between said patterned metal layer and the layer underneath, an annealing step is used

after said patterned metal layer is formed.

16. The method of claim 1, in which said catalyst-surfactant is Iodine or Iodine containing compound and said metal layer is copper layer.

17. The method of claim 16, in which in supplying Iodine or Iodine containing compounds into a CVD apparatus in order to treat said seed layer with catalyst-surfactants, said catalyst-surfactants contain Iodine and Iodine containing compounds including iodoethane(C_2H_5I), iodomethane(CH_3I), diiodomethane(CH_2I_2) and trifluoroiodmethane(CF_3I).

18. The method of claim 16; in which the materials that may be used as a seed layer are a metal group consisting of Copper(Cu), Titanium(Ti), Gold(Au), Silver(Ag), Palladium(Pd), Tungsten(W), Platinum(Pt) and Aluminum(Al), or a combination of one or more elements of the above.

19. The method of claim 16, in which a diffusion barrier layer is formed on said patterned insulation layer before said sees layer is formed.

20. The method of claim 16, in which Cu(I)-hexafluoroacetylacetonate vinyltrimethylsilane [(hfac)Cu(vtms)] is used as a copper source material for depositing copper by means of a CVD method using catalyst-surfactant.

21. The method of claim 16, in which the operating temperature of a CVD apparatus for depositing metal film layer is set at lower than 200 °C.

22. The method of claim 16, in which said depressions include contact holes that expose contain diffused areas in said substrate so that electrical interconnects can be made

in order to make semiconductor elements functional.

23. The method of claim 16, in which said depressions include via holes.

24. The method of claim 16, in which said depressions include trenches.

25. The method of claim 16, in which said depressions include contact holes and trenches.

26. The method of claim 16, in which said depressions include via holes and trenches.

27. The method of claim 19, in which before said diffusion barrier layer is formed, a refractory metal layer is formed on said patterned insulation layer.

28. The method of claims 16 or 18, in which in forming said seed layer, anisotropic deposition method is used in order to suppress said seed layer from being deposited on the sidewalls of said patterned depressions.

29. The method of claim 28, in which a collimated sputtering process is used as said anisotropic deposition method.

30. The method of claims 16 or 18, in which in forming said seed layer, anisotropic deposition method and isotropic etching method are used repeatedly at least once.

31. The method of claim 30, in which said collimated sputtering process is used as said anisotropic deposition method.

32. The method of claim 16, in which during the formation of said patterned copper film layer, a chemical-mechanical

polishing (CMP) method is used.

33. The method of claim 16 or 19, in which after said copper film layer is formed, an annealing process is used in order to enhance the adhesive characteristics between said patterned copper film layer and the layers underneath.

34. A method of forming metal interconnects comprising the steps of and in the order of:

forming an insulation layer on a top surface of a substrate;

forming a pattern of depressions in said insulation layer by etching;

forming a seed layer on the entire surface of said patterned insulation layer while suppressing formation of a seed layer on the sidewalls of said depressions;

removing said seed layer from the top flat part of the surface of said insulation layer;

treating a catalyst-surfactant on said surface of said seed layer; and

forming a metal layer on said patterned seed layer and said depressions from bottom up by means of a metal chemical vapor deposition (CVD) using catalyst-surfactant.

35. The method of claim 34, in which the materials that may be used as a seed layer are a metal group consisting of Copper(Cu), Titanium(Ti), Gold(Au), Silver(Ag), Palladium(Pd), Tungsten(W), Platinum(Pt) and Aluminum(Al), or a combination of one or more elements of the above.

36. The method of claim 34, in which during the process of removing said seed layer from the top flat part of the surface of said insulation layer, a chemical-mechanical polishing(CMP) method is used.

37. The method claim 36, in which a liquid solution not

containing solid particles is used as a polishing agent for chemical-mechanical polishing (CMP) operation.

38. The method of claim 19 or 34, in which before said seed layer is formed, an adhesive metal layer is formed in order to enhance the adhesive characteristics between said copper layer and said insulation layer or between said copper layer and said diffusion barrier layer.

39. The method of claim 34, in which said catalyst-surfactant is Iodine or Iodine containing compound and said metal layer is copper layer.

40. The method of claim 39, in which said chemicalmechanical polishing (CVD) method is used for removing said seed layer on the top flat part of said insulation layer.

41. The method of claim 40, in which a liquid solution not containing solid particles is used as a polishing agent for said chemical-mechanical polishing(CMP) operation.

Fig. 1A

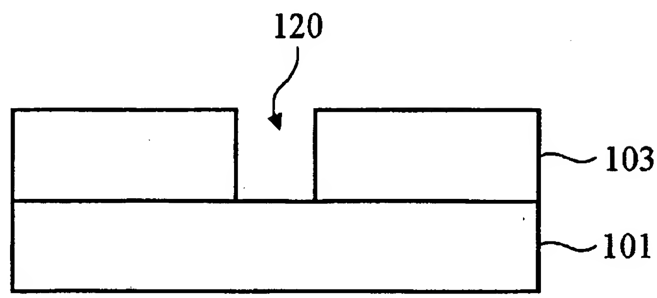


Fig. 1B

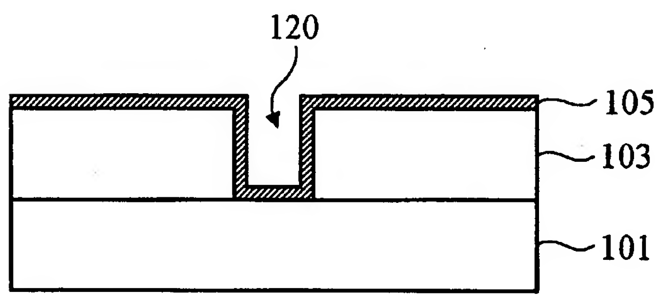


Fig. 1C

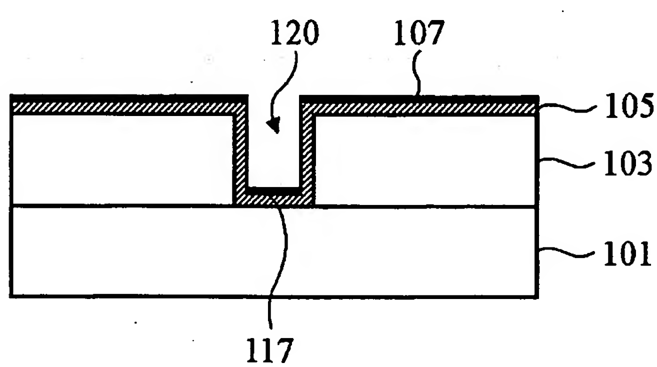


Fig. 1D

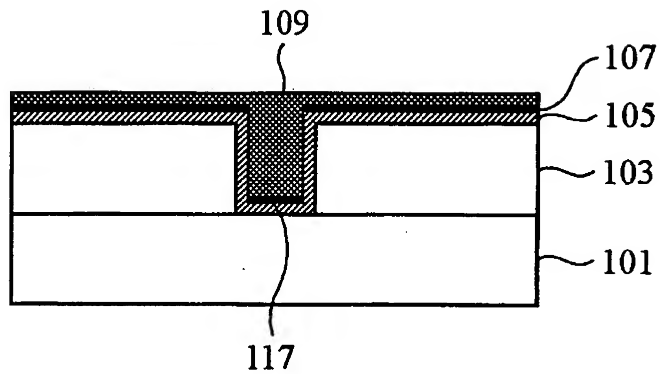


Fig. 1E

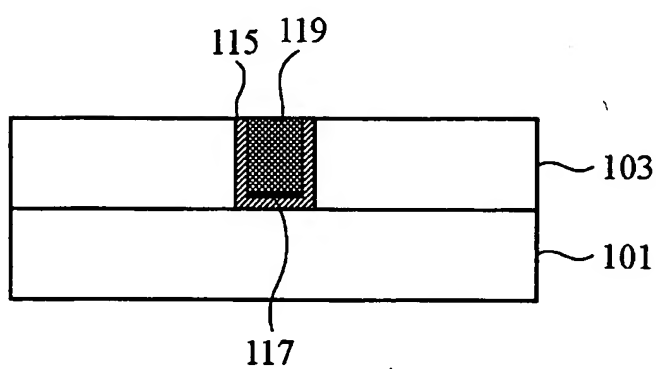


Fig. 2A

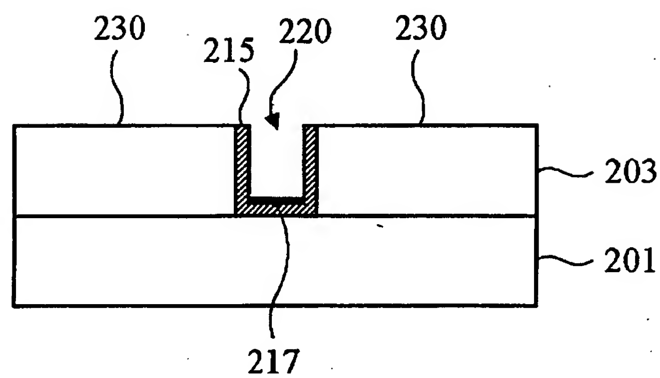
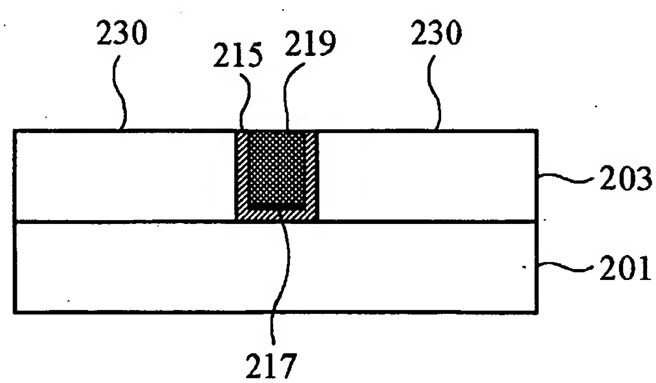


Fig. 2B



INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR 01/00605

CLASSIFICATION OF SUBJECT MATTER

IPC^7: H01L 21/285; 23/532; C23C 16/06; 16/44

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC^7: H01L; C23C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI; EPODOC; PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
E X	WO 01/45149 A1 (GENITECH CO LTD) 21 June 2001 (21.06.01) *the whole document.*	1-41
P,X	EP 1018758 A1 (SONY CORP) 12 July 2000 (12.07.00) *the whole document.*	1-41
A	WO 00/15866 A1 (GENITECH CO LTD) 23 March 2000 (23.03.00) *the whole document.*	1-41
A	WO 00/13207 A2/3 (GENITECH CO LTD) 9 March 2000 (09.03.00) *the whole document.*	1-41
A	US 5087485 A (TEXAS INSTRUMENTS INC (CHO CHIH-CHEN)) 11 February 1992 (11.02.92) *the whole document.*	1-41

☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

„A" document defining the general state of the art which is not considered to be of particular relevance

„E" earlier application or patent but published on or after the international filing date

„L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

„O" document referring to an oral disclosure, use, exhibition or other means

„P" document published prior to the international filing date but later than the priority date claimed

„T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

„X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

„Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

„&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
7 August 2001 (07.08.2001)	30 August 2001 (30.08.2001)

Name and mailing adress of the ISA/AT	Authorized officer
Austrian Patent Office Kohlmarkt 8-10; A-1014 Vienna Facsimile No. 1/53424/535	HEINICH Telephone No. 1/53424/454

Form PCT/ISA/210 (second sheet) (July 1998)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR 01/00605

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0234593 B1 (DOW CORNING) 20 May 1992 (20.05.92) *the whole document.*	1-41
A	JP 08 250438 A (RES DEV CORP OF JAPAN) 27 September 1996 (27.09.96) *the whole document.*	1-41

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/KR 01/00605

Patent document cited in search report			Publication date	Patent family member(s)			Publication date
EP	A2	234593	02-09-1987	CA	A1	1303915	23-06-1992
EP	A3	234593	31-08-1988	DE	C0	3779144	25-06-1992
EP	B1	234593	20-05-1992	JP	A2	62249415	30-10-1987
				US	A	4696834	29-09-1987
EP	A1	1018758	12-07-2000	JP	A2	00223419	11-08-2000
				WO	A1	00001005	06-01-2000
JP	A2	8250438	27-09-1996			none	
US	A	5087485	11-02-1992			none	
WO	A	0013207				none	
WO	A	0015866				none	
WO	A	0145149				none	